DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

LIST OF COURSES OFFERED FOR HONOR PROGRAM (R20)

Course code	Course Title	Contact hours/week				Credits
		L	T	P	**Total**	
20ECH1	CPLD And FPGA Architectures	3	1	0	4	4
20ECH2	Real Time Operating Systems	3	1	0	4	4
20ECH3	VLSI Design Automation	3	1	0	4	4
20ECH4	VLSI Testing and Verification	3	1	0	4	4

B.Tech. (IV Sem)	20ECH1-CPLD and FPGA Architectures	L	T	P	Cr.
		3	1	0	4

Pre-Requisites: Basics on CPLD and FPGA

COURSE EDUCATIONAL OBJECTIVES:

In this course student will learn about the complex programmable logic devices, field programmable gate arrays, architecture of SRAM programmable and anti-fuse programmed FPGAs.

COURSE OUTCOMES: At the end of this course student will be able to

CO1 **Analyze** different types of Complex Programmable Logic Devices.
CO2 **Understand** different types of Field Programmable Gate Arrays.
CO3 **Evaluate** architecture of SRAM Programmable FPGAs.
CO4 **Explain** the device Architecture of Anti-Fuse Programmed FPGAs.
CO5 **Design** the application for Combinational and Sequential Circuits.

UNIT - I:

Introduction to Programmable Logic Devices:

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic.

UNIT – II:

Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD Implementation of a Parallel Adder with Accumulation. Altera series – Max 5000/7000 series, Altera FLEX logic-10000 series CPLD.

UNIT – III:

Field Programmable Gate Arrays:

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated specialized Components of FPGAs, and Applications of FPGAs.

UNIT – IV:

SRAM Programmable FPGAs:

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000, XC4000 Architectures.

Anti-Fuse Programmed FPGAs:

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT – V:

Design Applications:

General Design Issues, Counter Examples, A Fast Video Controller, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXTBOOKS

1. Field Programmable Gate Array Technology by Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design by Charles H. Roth Jr, LizyKurian John, Cengage Learning.

REFERENCES:

1. Field Programmable Gate Arrays by John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays by Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs by Ian Grout, Elsevier, Newnes.
4. FPGA based System Design by Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

B.Tech. (V Sem.)	20ECH2-Real Time Operating Systems	L	T	P	Cr.
		3	1	0	4

PRE-REQUISITES: Embedded System Design

COURSE EDUCATIONAL OBJECTIVES:

In this course student will learn about fundamental concepts of real time operating systems, operating system objects, services and I/O concepts, various interrupts and timers.

COURSE OUTCOMES:

At the end of the course, student will be able to

CO1 **Understand** the basic set of commands and utilities in Linux/UNIX systems.
CO2 **Explain** the fundamental concepts of real-time operating systems.
CO3 **Analyze** real-time operating systems objects, services and I/O concepts.
CO4 **Evaluate** various Interrupts and Timers.
CO5 **Design** real time embedded systems using the concepts of RTOS.

UNIT – I:

Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II:

Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, Tasks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III:

Objects, Services and I/O Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV:

Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT V:

RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

TEXT BOOKS:

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011

REFERENCE BOOKS:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

B.Tech. (VI Sem.) **20ECH3-VLSI Design Automation**

L	T	P	Cr.
3	1	0	4

Pre-Requisites: VLSI Design

COURSE EDUCATIONAL OBJECTIVES:

In this course student will learn about the design cycles, various techniques on Partitioning, Placement and Routing and addressing their problems.

COURSE OUTCOMES: At the end of this course student will be able to

CO1: Understand need for VLSI physical design automation.

CO2: Analyze VLSI automation algorithms for partitioning.

CO3: Formulate placement, floor planning and pin assignment problems and simulate.

CO4: Resolve routing issues using various algorithms.

CO5: Illustrate physical design cycle for FPGAs.

UNIT I:

VLSI Physical Design Automation: Introduction, VLSI Design cycle, new trends in VLSI design cycle, new trends in Physical design cycle, Design styles, full custom Basic terminology, complex issues, basic algorithms, Basic data structures, and algorithms.

UNIT II:

VLSI Automation Algorithms: Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

UNIT III:

Placement, Floor Planning & Pin Assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment

UNIT IV:

Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches

Detailed Routing: Problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

Over The Cell Routing & Via Minimization: two layers over the cell routers, constrained & unconstrained via minimization

UNIT V:

Physical design Automation of FPGAs:

Introduction, FPGA Technologies, Physical design cycle for FPGAs, Partitioning, Routing, Routing algorithms for the non-segmented model, Routing algorithms for segmented model, routing algorithms for staggered model.

TEXT BOOK:

1. Naveed Shervani, **"Algorithms for VLSI Physical Design Automation"**, Springer Publisher, Third edition.

REFERENCE BOOKS:

1. ChristophnMeinel& Thorsten Theobold, **"Algorithm and Data Structures for VLSI Design"**, KAP, 2002.
2. Rolf Drechsheler :**"Evolutionary Algorithm for VLSI"**, Second edition.
3. Trimburger, **"Introduction to CAD for VLSI",** Kluwer Academic publisher, 2002.

B.Tech. (VII Sem.)	20ECH4-VLSI Testing and Verification	L	T	P	Cr.
		3	1	0	4

PRE-REQUISITES: None

COURSE EDUCATIONAL OBJECTIVES:

In this course student will learn about testable design, test generation algorithms for combinational and sequential circuits, design verification and verification tools, timing and physical design verification.

COURSE OUTCOMES:

At the end of the course, student will be able to

CO1 Identify the significance of testable design
CO2 Implement combinational and sequential circuit test generation algorithms
CO3 Understand the importance of Design verification.
CO4 Learn verification tools.
CO5 Analyze the static timing verification and physical design verification.

UNIT I:

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends Affecting Testing. Faults in Digital Circuits: Failures and Faults, Modelling of Faults, Temporary Faults.

Test Generation for Combinational Logic Circuits: Fault Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits, Detection of Multiple Fauls in Combinational Logic Circuits.

UNIT II:

Design of Testable Sequential Circuits: Controllability and Observability, Ad Hoc Design Rules for Improving Testability, Design of Diagnosable Sequential Circuits, The Scan-Path Technique for Testable Sequential Circuit Design, Level-Sensitive Scan Design, Random Access
Scan Technique, Partial Scan, Testable Sequential Circuit Design Using Non-scan Techniques, Cross Check, Boundary Scan. Built-In Self Test: Test Pattern Generation for BIST, Output Response Analysis, Circular BIST, BIST Architectures.

UNIT III:

Testable Memory Design: RAM Fault Models, Test Algorithms for RAMs, Detection of Pattern Sensitive Faults, BIST Techniques for Ram Chips, Test Generation and BIST for Embedded RAMs.
Importance of Design Verification: What is verification? What is attest bench? The importance of verification, Reconvergence model, Formal verification, Equivalence checking, Model checking, Functional verification.[Ref4- Chapter1]

UNIT IV:

Verification Tools: Linting tools: Limitations of linting tools, linting verilog source code, linting VHDL source code, linting OpenVera and esource code, code reviews. Simulators: Stimulus and response, Event based simulation, cycle based simulation, Co-simulators, verification intellectual property: hardware modelers, waveform viewers.[Ref4-Chapter2]

The verification plan: The role of verification plan: specifying the verification plan, defining the first success. Levels of verification: unit level verification, reusable components verification, ASIC

and FPGA verification, system level verification, board level verification, verifying strategies, verifying responses. [Ref4-Chapter3]

UNIT V:

Static Timing Verification: Concept of static timing analysis. Cross talk and noise. Limitations of STA. slew of a wave form, Skew between the signals, Timing arcs and unateness, Min and Max timing paths, clock domains, operating conditions, critical path analysis, false paths, Timing models. [Ref5 Chapter 1, 2, 3, 8]

Physical Design Verification: Layout rule checks and electrical rule checks. Parasitic extraction. Antenna, Crosstalk and Noise**:** Cross talk glitch analysis, crosstalk delay analysis, timing verification [Ref6 Chapter 8]

TEXT BOOKS:

1. P. K. Lala, **"Digital Circuit Testing and Testability"**, Academic Press
2. M.L. Bushnell and V.D. Agrawal, **"Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits"**, Kluwar Academic Publishers.

REFERENCE BOOKS:

1. M. Abramovici, M.A. Breuer and A.D. Friedman, **"Digital Systems and Testable Design"**, Jaico Publishing House, 2002.
2. Janick Bergeron, **"Writing test benches: functional verification of HDL models"**, 2nd edition ,Kluwer Academic Publishers,2003
3. Jayaram Bhasker, RakeshChadha, **"Static Timing Analysis for Nanometer Designs"** A practical approach, Springer publications
4. Prakash Rashinkar, Peter Paterson, Leena Singh **"System on a Chip Verification"**, Kulwer Publications.